REMARKS

The claims are claims 2, 4, 5 and 11.

The Notice of Non-Compliant Amendment indicated that all pages of the response filed March 24, 2006 were not received by the U.S. Patent and Trademark Office. The inadvertently omitted pages included: the end of the amendment to the specification at paragraph at page 19, lines 15 to 28; amendment to the specification at page 20, line 12 to page 21, line 9; amendment to the specification at page 21, lines 10 to 26; amendment to the specification at page 56, line 1 as follows; a complete listing of the claims including the changes noted below; and the arguments included below.

Claims 4 and 5 are amended. Claim 3 is newly canceled. New claim 11 is added. Claim 4 is amended to incorporate the digital signal processor limitation of canceled claim 3 and to include additional limitations on the successive midpoint approximation described in the application at page 54, line 23 to page 57, line 2 and illustrated in Figure 24. Claim 5 is amended to incorporate the reduced instruction set processor limitation of canceled claim 3 and to include additional limitations on the edge intersection calculation described in the application at page 53, line 13 to page 54, line 22 and illustrated in Figure 23. New claim 11 recites subject matter not previously claimed described in the application at page 61, line 5 to page 63, line 13 and illustrated in Figure 28.

Claims 2 to 5 were rejected under the judicially created doctrine of double patenting over claims 1 to 5 of Gupta et al U.S. Patent No. 6,693,719. The OFFICE ACTION states the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter. The OFFICE ACTION states that claims 2 to 5 of the patent make obvious the limitations of claims 2 to 5 of this application. The OFFICE ACTION further states there is

no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent.

The Applicants respectfully submit that this double patenting rejection is improper and should be withdrawn. This application is a divisional of U.S. Patent Application Serial No. 09/397,540 that matured into U.S. Patent No. 6,693,719. That prior application Serial No. 09/397,540 was subject to a telephonic restriction requirement on September 24, 2003. The OFFICE ACTION states there is no apparent reason why the present claims were not presented in the prior application. In fact, the current claims 2 to 5 were presented in the prior application but were canceled in response to the telephonic restriction requirement. According to 35 U.S.C. 121 a obviousness type double patenting rejection to this application claiming non-elected subject matter in the parent application is improper.

Claim 2 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Easwar et al U.S. Patent No. 6,101,290 and Dye et al U.S. Patent No. 6,518,965.

Claim 2 recites subject matter not made obvious by the combination of Easwar et al and Dye et al. Claim 2 recites "spawning a subtask from said first processor to another of said processors." The OFFICE ACTION cites column 2, lines 62 to 65 of Easwar et al as making obvious this subject matter. Easwar et al states at column 2, lines 62 to 65:

> "The invention is useful with any multiprocessor system, that is, a system where multiple processors share raster image processing tasks and use a common bus, operating concurrently and not necessarily on the same task at once."

This discloses multi-processing but fails to teach spawning a process from one processor to another. Thus claim 2 is allowable over the combination of Easwar et al and Dye et al.

Claim 2 recites further subject matter not made obvious by the combination of Easwar et al and Dye et al. Claim 2 recites "sorting polygon edges in increasing minimum Y coordinate." The OFFICE ACTION cites Dye et al at column 28, lines 28 to 42 as anticipating this subject matter. Dye et al states at column 22, lines 28 to 42 (including the portion of cited in the OFFICE ACTION):

> "Multiple cases exist for triangle parameterization. One case is when the main slope is left of the apex (mid point) vertex of the triangle, and a second is when the main slope is to the right of the apex point. Also, during the triangle parameterization flat top and flat bottom, single-scan line, and single-point cases are also detected for additional efficiency. In the preferred embodiment, it is desirable to only carry the minimum number of parameters to complete the entire polygon parameterization as required by the rasterization process. In order to start the parameterization process, the execution engine first performs a quick position sort of the triangle to find the top and mid vertex. This conventional operation finds the minimum X and Y coordinate positions. From this information each of the two cases mentioned above can be identified. The easy case, for example, is when the main slope of a triangle is on the left of the mid vertex position. In this case the slope increment values for the positions and depths for the main and opposite edges are calculated and stored in a vertex array along with pointers to the remaining parameters required for completion of the set-up process."

The sorting disclosed in this portion of Dye et al does not make obvious the sorting recited in claim 2. This portion of Dye et al teaches "a quick position sort of the triangle to find the top and mid vertex." The sorting recited in claim 2 is of polygon edges in increasing minimum Y coordinate. Thus this recitation of claim 2 requires plural polygons while the sorting of Dye et al concerns finding top and bottom edges of a single triangle. Accordingly

claim 2 is allowable over the combination of Easwar et al and Dye et al.

Claim 2 is further unobvious over Easwar et al and Dye et al. Easwar et al discloses a multiprocessor without disclosing the particular processes (1 interpreting the page and 2 sorting polygon edges in increasing minimum Y coordinate) recited in claim 2. Dye et al arguably teaches sorting polygon edges without teaching a multiprocessor. The Applicants respectfully submit that while Easwar et al teaches division of tasks between processors of a multiprocessor, it fails to make obvious the particular division of tasks claimed. Dye et al teaches these tasks without any teaching that they can be divided in the manner claimed. Accordingly, one skilled in the art would not make the particular task division recited in claim 2 absent the teaching of this application. Accordingly, claim 2 is allowable over the combination of Easwar et al and Dye et al.

Claims 4 and 5 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Easwar et al U.S. Patent No. 6,101,290, Dye et al U.S. Patent No. 6,518,965 and Inoue et al U.S. Patent No. 5,974,436.

Claim 4 recites subject matter not made obvious by the combination of Easwar et al, Dye et al and Inoue et al. Claim 4 recites "detecting a Y coordinate of edge intersection via successive midpoint approximation." The OFFICE ACTION cites column 28, lines 28 to 42 of Dye et al as making obvious this limitation. However, this portion of Dye et al fails to teach successive approximation in any form. This portion of Dye et al likewise includes no teaching of midpoint approximation. The portion of Dye et al cited in the OFFICE ACTION uses the mid vertex position to evaluate the slope of the line. This fails to calculate the Y coordinate of the edge intersection as claimed. Claim 4 includes further details of the successive midpoint approximation that are

not shown in Easwar et al, Dye et al or Inoue et al. Accordingly, claim 4 is allowable over the combination of Easwar et al, Dye et al and Inoue et al.

Claim 5 recites subject matter not made obvious by the combination of Easwar et al, Dye et al and Inoue et al. Claim 5 recites "calculating a Y coordinate of edge intersection employing said floating point calculation unit of said first processor." Dye et al teaches intersection calculation without teaching this calculation employs a floating point calculation unit. Inuoe et al teaches a floating point calculation unit without teaching the edge intersection calculation claimed. Claim 5 further includes details of this calculation that are not shown in Easwar et al, Dye et al or Inoue et al. Accordingly, claim 5 is allowable over the combination of Easwar et al, Dye et al and Inoue et al.

New claim 11 recites subject matter not made obvious by the combination of Easwar et al, Dye et al and Inoue et al. Claim 13 recites "forming a queue of parallel tasks with said first processor; and dispatching a parallel task from said queue to a next available other processor." The Applicants respectfully submit that the combination of Easwar et al, Dye et al and Inoue et al fail to make obvious the queue of parallel tasks and likewise fail to make obvious dispatching tasks in the queue to a next available processor. Accordingly, claim 11 is allowable over the combination of Easwar et al, Dye et al and Inoue et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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